What is claimed is:

1. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

2. A camera device as in claim 1 wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors substantially simultaneously.

Sub C2

3. A camera device as in claim 1, further comprising double sampling charge storage elements on said substrate.

4. A camera device as in claim 1, wherein said timing circuit includes a timer for first sampling a reset level on a first of said charge storage elements, and then for second sampling a signal level on a second of said charge storage elements.

Sub D1

5. A camera device as in claim 2 further comprising a plurality of double sampling charge storage elements integrated on said substrate; one for each of said columns.

6. A camera device as in claim 5, wherein said timing circuit includes a timer for first sampling all reset levels in a specific column on first charge storage elements, and then for second sampling all signal levels on second charge storage elements.

Sub D2

7. A camera device as in claim 1, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

A camera device as in claim 5, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

9. A camera device as in claim 1, wherein said photoreceptors are photodiodes.

10. A camera device as in claim 1, wherein said photoreceptors are photogates.

11. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

12. A camera device as in claim 11, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

13. A camera device as in claim 11, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

14. A camera device as in claim 13, wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

15. A camera device as in claim 13, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

16. A camera device as in claim 15, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

17. A camera device as in claim 11, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

18. A camera device as in claim 17, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

19. A camera device as in claim 17, wherein said photoreceptors are photodiodes.

20. A camera device as in claim 17, wherein said photoreceptors are photogates.

21. A camera device as in claim 11, further comprising a mode selector device, selecting a mode of operation of said chip.

22. A camera device as in claim 21, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

23. A camera device as in claim 11, further comprising a correlated double sampling circuit.

24. A camera device as in claim 11, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

25. A camera device as in claim 22, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

26. A camera device as in claim 11, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

27. A camera device as in claim 11, further comprising fixed pattern noise reduction circuits, on said substrate.

28. A camera device as in claim 11, further comprising a double delta sampling element integrated on the chip, which shorts sampled signals during the readout cycle reducing column fixed pattern noise.

29. A camera device as in claim 11, further comprising a noise reduction circuit.

30. A camera device as in claim 11, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

19
31. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors.

20 19
32. A camera device as in claim 31, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

33. A camera device as in claim 32, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

34. A camera device as in claim 31 further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop values.

35. A camera device as in claim 31, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

36. A camera device as in claim 35, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

37. A camera device as in claim 31, wherein said photoreceptors are photodiodes.

38. A camera device as in claim 31, wherein said photoreceptors are photogates.

25 19
39. A camera device as in claim 31, wherein said photoreceptors are either photogates or photodiodes, further comprising a mode selector device which selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

27 19
40. A camera device as in claim 31, further comprising a correlated double sampling circuit integrated on the chip.

28 19
41. A camera device as in claim 31, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

26 25
42. A camera device as in claim 39, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

Sub cl
43. A camera device as in claim 31, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

~~44~~. A camera device as in claim 31, further comprising a noise reduction circuit.

~~45~~ 33. A camera device as in claim ~~44~~ 32, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

~~46~~ 34. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used.

47. A camera device as in claim 46, wherein said photoreceptor is one of a photodiode or a photogate, and said array is controlled into said first mode for said photogate and in said second mode for said photodiode.

48. A camera device as in claim 46, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

49. A camera device as in claim 48, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

50. A camera device as in claim 47, further comprising a correlated double sampling circuit.

51. A camera device as in claim 47, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

52. A camera device as in claim 47, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

53. A camera device as in claim 46 further comprising a noise reduction circuit.

54. A camera device as in claim 52, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

55. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of

operation of said array of photoreceptors to read at least one element of the array by first reading a reset level of said at least one element, and subsequently, after an integration time, second reading a charged level of said at least one photoreceptor, said reading and said second reading producing output signals based on both said charged level and said reset level.

56. A single chip camera device as in claim 55 wherein an output signal is equal to said charged level minus said reset level.

57. A camera device as in claim 55, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

58. A camera device as in claim 55, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

59. A camera device as in claim 58, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

60. A camera device as in claim 58, wherein said photoreceptors are photodiodes.

61. A camera device as in claim 58, wherein said photoreceptors are photogates.

62. A camera device as in claim 55, further comprising a mode selector device, selecting a mode of operation of said chip.

63. A camera device as in claim 62, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

64. A camera device as in claim 63, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

65. A camera device as in claim 55, wherein said timing circuit allows changing an integration time for said array of photoreceptors by changing a time interval between said first and second reading.

66. A camera device as in claim 55, further comprising fixed pattern noise reduction circuits, on chip.

67. A camera device as in claim 55, further comprising a noise reduction circuit.

68. A camera device as in claim 67, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

69. A camera device as in claim 67, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

70. A camera device as in claim 67, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

71. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors; and

a circuit, integrated on said substrate, which reduces a fixed pattern noise.

72. A camera device as in claim 71, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

73. A camera device as in claim 71, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

74. A camera device as in claim 73, wherein said readout amplifier is preferably within and/or associated with one element of the array.

75. A camera device as in claim 73, wherein said photoreceptors are photodiodes.

76. A camera device as in claim 73 wherein said photoreceptors are photogates.

77. A camera device as in claim 71, further comprising a mode selector device, selecting a mode of operation of said chip.

09120355 . 072105

78. A camera device as in claim 77, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

79. A camera device as in claim 71, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

80. A camera device as in claim 78, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

81. A camera device as in claim 71, wherein said circuit that reduces fixed pattern noise includes at least one charge storage device, sampling a level indicative of reset.

82. A camera device as in claim 71, wherein said circuit that reduces fixed pattern noise includes at least two charge storage devices, one controlled by said timing circuit to first sample a level indicative of reset, and another controlled by said timing circuit to second sample a level indicative of a charged device.

83. A camera device as in claim 82, further comprising a shorting element that shorts together said two charge storage devices prior to sampling said reset level.

84. A camera device as in claim 82, wherein said timing circuit allows changing an integration time for said array of photoreceptors by changing a time between said first sample and said second sample.

85. A camera device as in claim 85, wherein said timing circuit times an operation of said fixed pattern noise reduction circuit to occur during a time of the video signal which is not being displayed.

86. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control row and address decoders and delay counters.

87. A camera device as in claim 86, wherein said signal controlling device includes a column-parallel read out device, which reads out a column of said photoreceptors at substantially the same time.

88. A camera device as in claim 43, wherein said signal controlling device includes a column selector allowing selection of a desired row for read out, and a row selector which allows selection of a desired row for readout.

89. A camera device as in claim 49 wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

90. A camera device as in claim 49, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

91. A camera device as in claim 90, further comprising an input data bus, connected to the camera device, values on said data bus being used to preset said start and stop column decoder counters.

92. A camera device as in claim 86, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

93. A camera device as in claim 92, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

94. A camera device as in claim 92, wherein said photoreceptors are photodiodes.

95. A camera device as in claim 92 wherein said photoreceptors are photogates.

96. A camera device as in claim 86, further comprising a mode selector device, selecting a mode of operation of said chip.

40 97. A camera device as in claim 59 96, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

51 98. A camera device as in claim 43 86, further comprising a correlated double sampling circuit.

58 99. A camera device as in claim 43 86, wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

61 100. A camera device as in claim 60 97, further comprising a differencing mode which alters readout timing in such a way that the value of each pixel output represents a difference between a current frame and a previous frame.

Sub CG 70 101. A camera device as in claim 86, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

102. A camera device as in claim 87, further comprising a noise reduction circuits, on chip.

103. A camera device as in claim 102, wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

104. A camera device as in claim 102, wherein said noise reduction circuit is a fixed pattern noise reduction circuit.

105. A camera device as in claim 102, wherein said noise reduction circuit is a column to column fixed pattern noise reduction circuit.

106. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously.

76 75
~~107~~. A device as in claim ~~106~~, wherein said logic elements control said pixels to first sample a reset level of each said row, and then to sample a charged level of said charge storage elements to produce information indicating a correlated signal indicative of a difference therebetween.

77 75
~~108~~. A device as in claim ~~106~~, wherein said control portion includes a plurality of column selection p-channel transistors, respectively associated with each column, said transistors being turned on to sample a column.

78 75
~~109~~. A device as in claim ~~106~~, wherein there is one of said charge storage elements associated with each of said columns.

79 75
~~110~~. A device as in claim ~~106~~, wherein there are two of said charge storage elements associated with each of said columns.

80 75
~~111~~. A camera device as in ~~claim~~ ~~106~~, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

81 80
~~112~~. A camera device as ~~in claim~~ ~~111~~, wherein said readout amplifier is preferably within and/or associated with one element of the array.

82 80
~~113~~. A camera device as in claim ~~111~~, wherein said photoreceptors are photodiodes.

83 80
~~114~~. A camera device as in claim ~~111~~, wherein said photoreceptors are photogates.

65

115. A camera device as in claim 106, further comprising a mode selector device, selecting a mode of operation of said chip.

116. A camera device as in claim 106, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

117. A camera device as in claim 106, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

118. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including logic elements to control a double delta sampling, integrated on the chip, which shorts sampled signals during the readout cycle, thereby reducing column fixed pattern noise.

119. A camera device as in claim 118, wherein said signal controlling device includes a column-parallel read out device, which reads out a row of said photoreceptors at substantially the same time.

120. A camera device as in claim 118, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout.

121. A camera device as in claim 118, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

122. A camera device as in claim 121, wherein said readout amplifier is preferably within and/ or associated with one element of the array.

123. A camera device as in claim 121, wherein said photoreceptors are photodiodes.

124. A camera device as in claim 121, wherein said photoreceptors are photogates.

125. A camera device as in claim 118, further comprising a mode selector device, selecting a mode of operation of said chip.

126. A camera device as in claim 125, wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.

127. A camera device as in claim 118, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

128. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and control portion, both of which are formed using a logic family that is compatible with CMOS.

said image acquisition portion integrated in said substrate including an array of photoreceptors in rows and columns;

first and second charge storage elements, associated with each said column;

said control portion integrated in said substrate including a signal controlling device,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of

operation of said array of photoreceptors, controlling said photoreceptors to output their signals such that said first charge storage element receives the signal indicative of reset and said second charge storage element receives a signal indicative of a charged state;

said control portion including a shorting element, formed on said substrate which shorts between said first and second charge storage elements to reduce noise produced thereby.

129. A device as in claim 128, wherein said photoreceptors are controlled to read out an entire column of information at one time, wherein there are one of said first and second charge storage elements on said substrate for each element of said column, and wherein there is one of said shorting elements on said substrate for each of said columns.

130. A camera device as in claim 128, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

131. A camera device as in claim 130, wherein said readout amplifier is preferably within and/or associated with one element of the array.

132. A camera device as in claim 130, wherein said photoreceptors are photodiodes.

133. A camera device as in claim 130, wherein said photoreceptors are photogates.

134. A camera device as in claim 128, wherein said timing circuit allows changing an integration time for said array of photoreceptors with changing timings of said first and second charge storage elements.

135. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors, and a signal controlling device, controlling said

photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

determining a first mode of operation for said photoreceptors being photogates, and a second mode of operation for said photoreceptors being photodiodes;

using said on-chip timing and control circuit to control sequences for accessing rows in a specified order depending on said mode of operation, using a first sequence for said first mode of operation for photogates, and a second mode of operation for said second mode for photodiodes, a timing for said first mode being different than a timing for said second mode.

136. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors with output nodes, and a signal controlling

device, controlling said photoreceptors and a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

resetting said output nodes;

sampling a reset value as a first sample;

allowing said photoreceptors to accumulate charge, after resetting said output nodes;

sampling said output nodes after accumulating said charge, producing output signals indicative of a difference between said reset value and said sampled value after accumulating said charge.

137. A method in claim 137 wherein said reset level is sampled during a blanking interval of the video signal.

138. A method of controlling a single chip camera, comprising:

integrating, on a single substrate, an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS, said image acquisition portion integrated in said substrate including an array of photoreceptors with output nodes, and a signal controlling device, controlling said photoreceptors and a timing circuit

integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and also integrating at least two charge storage elements on said substrate;

first, shorting together specified nodes of said two charge storage elements;

after said first shorting, sampling voltages on said charge storage elements, said voltages being related to one another.

139. A method as in claim 138, further comprising:

sampling a reset value as a first sample;

allowing said photoreceptors to accumulate charge, after resetting said output nodes;

sampling said output nodes after accumulating said charge, producing output signals indicative of a difference between said reset value and said sampled value after accumulating said charge.

140. A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors and a noise reduction circuit;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors and controlling an operation of said noise reduction circuit to occur during a time when signals are not being read from said array of photodetectors.

09125595.072198